19-4796; Rev 1; 6/00

EVALUATION KIT AVAILABLE

1.25Gbps/2.5Gbps, +3V to +5.5V, Low-Noise Transimpedance Preamplifiers for LANs

General Description

The MAX3266 is a transimpedance preamplifier for 1.25Gbps local area network (LAN) fiber optic receivers. The circuit features 200nA input-referred noise, 920MHz bandwidth, and 1mA input overload.

The MAX3267 provides a pin-for-pin compatible solution for communications up to 2.5Gbps. It features 500nA input-referred noise, 1.9GHz bandwidth, and 1mA input overload.

Both devices operate from a +3.0V to +5.5V single supply and require no compensation capacitor. They also include a space-saving filter connection that provides positive bias for the photodiode through a 1.5kΩ resistor to V_{CC}. These features allow easy assembly into a TO-46 or TO-56 header with a photodiode.

The 1.25Gbps MAX3266 has a typical optical dynamic range of -24dBm to 0dBm in a shortwave (850nm) configuration or -27dBm to -3dBm in a longwave (1300nm) configuration. The 2.5Gbps MAX3267 has a typical optical dynamic range of -21dBm to 0dBm in a shortwave configuration or -24dBm to -3dBm in a longwave configuration.

Applications

Gigabit Ethernet

1Gbps to 2.5Gbps Optical Receivers

Fibre Channel

Features

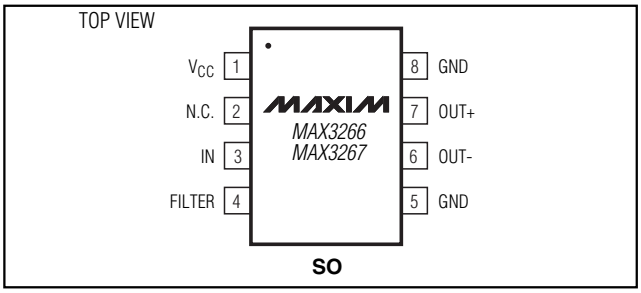
- **200nA Input-Referred Noise (MAX3266)**
  500nA Input-Referred Noise (MAX3267)
- **920MHz Bandwidth (MAX3266)**
  1900MHz Bandwidth (MAX3267)
- **1mA Input Overload**
- **+3.0V to +5.5V Single-Supply Voltage**

Ordering Information

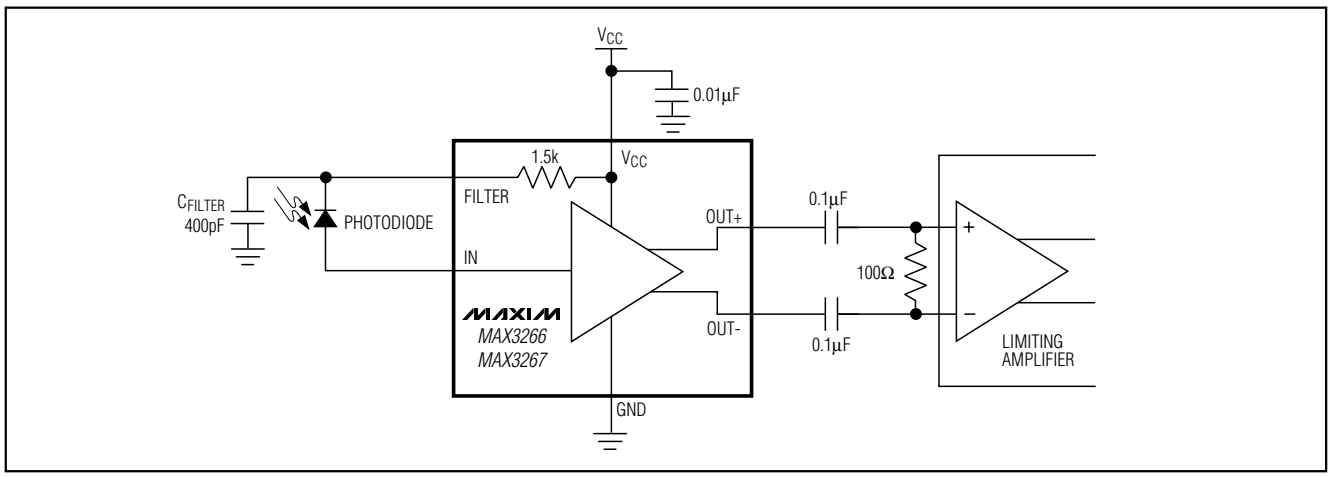
PART	TEMP. RANGE	PIN-PACKAGE
MAX3266CSA	0°C to +70°C	8 SO
MAX3266C/D	—	Dice*
MAX3267CSA	0°C to +70°C	8 SO
MAX3267C/D	—	Dice*
MAX3267ESA	-40°C to +85°C	8 SO
MAX3267E/D	—	Dice*

**Dice are designed to operate over a -40°C to +140°C junction temperature (Tj) range, but are tested and guaranteed at T_A = +25°C.*

Pin Configuration



Typical Application Circuit



1.25Gbps/2.5Gbps, +3V to +5.5V, Low-Noise Transimpedance Preamplifiers for LANs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - GND) .....-0.5V to +6.0V
IN Current.....-4mA to +4mA
FILTER Current.....-8mA to +8mA
Voltage at OUT+, OUT- .....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 6.7mW/°C above +70°C).....533mW
Storage Temperature Range .....-55°C to +150°C
Operating Junction Temperature (die) .....-55°C to +150°C
Processing Temperature (die) .....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX3266C/MAX3267C

(V_{CC} = +3.0V to +5.5V, T_A = 0°C to +70°C, 100Ω load between OUT+ and OUT-. Typical values are at T_A = +25°C, V_{CC} = 3.3V, source capacitance = 0.85pF, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Voltage			0.69	0.83	0.91	V
Supply Current				26	50	mA
Transimpedance	Differential, measured with 30µAp-p signal (40µAp-p for MAX3267)	MAX3266	2260	2800	3400	Ω
		MAX3267	1540	1900	2330	
Output Impedance	Single ended (per side)		48	50	52	Ω
Maximum Differential Output Voltage	Input = 1mAp-p		185	250	415	mVp-p
Filter Resistor			1220	1500	1860	Ω
AC Input Overload			1.0			mAp-p
DC Input Overload			0.65			mA
Input-Referred RMS Noise	Die, packaged in TO-56 header (Note 2)	MAX3266		192	256	nA
	SO package (Note 2)	MAX3266		200		
		MAX3267		485	655	
Input-Referred Noise Density	(Note 2)	MAX3266		6.6		pA/(Hz)$^{1/2}$
		MAX3267		11.0		
Small-Signal Bandwidth	MAX3266		750	920	1100	MHz
	MAX3267		1530	1900	2420	
Low-Frequency Cutoff	-3dB, input ≤ 20µA DC			44		kHz
Transimpedance Linear Range	Peak-to-peak, 0.95 < linearity < 1.05	MAX3266	30			µAp-p
		MAX3267	40			
Deterministic Jitter	(Note 3)	MAX3266		19	76	ps
		MAX3267		12	50	
Power-Supply Rejection Ratio (PSRR)	Output referred, f < 2MHz, PSRR = -20log ($\Delta V_{OUT}/\Delta V_{CC}$)			50		dB

ELECTRICAL CHARACTERISTICS—MAX3267E

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, 100Ω load between OUT+ and OUT-. Typical values are at T_A = +25°C, V_{CC} = 3.3V, source capacitance = 0.85pF, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage		0.67	0.83	0.97	V
Supply Current			26	53.2	mA
Transimpedance	Differential, measured with 40µAp-p signal	1470	1900	2355	Ω
Output Impedance	Single ended (per side)	47.7	50	52.1	Ω
Maximum Differential Output Voltage	Input = 1mAp-p	155	250	430	mVp-p
Filter Resistor		1210	1500	1865	Ω
AC Input Overload		1.0			mAp-p
DC Input Overload		0.65			mA
Input-Referred RMS Noise	SO package (Note 2)		485	668	nA
Input-Referred Noise Density	(Note 2)		11.0		$pA/(Hz)^{1/2}$
Small-Signal Bandwidth		1515	1900	2550	MHz
Low-Frequency Cutoff	-3dB, input ≤ 20µA DC		24		kHz
Transimpedance Linear Range	Peak-to-peak, 0.95 < linearity < 1.05	40			µAp-p
Deterministic Jitter	(Note 3)		14	50	ps
Power-Supply Rejection Ratio (PSRR)	Output referred, f < 2MHz, PSRR = -20log ($\Delta V_{OUT}/\Delta V_{CC}$)		50		dB

Note 1: Source Capacitance represents the total capacitance at the IN pin during characterization of noise and bandwidth parameters. Figure 1 shows the typical source capacitance vs. reverse voltage for the photodiode used during characterization of TO-56 header packages. Noise and bandwidth will be affected by the source capacitance. See the *Typical Operating Characteristics* for more information.

Note 2: Input-Referred Noise is calculated as RMS Output Noise / (Gain at f = 10MHz). Noise Density is (Input-Referred Noise) / $\sqrt{\text{bandwidth}}$. No external filters are used for the noise measurements.

Note 3: Deterministic Jitter is measured with the K28.5 pattern applied to the input [00111110101100000101].

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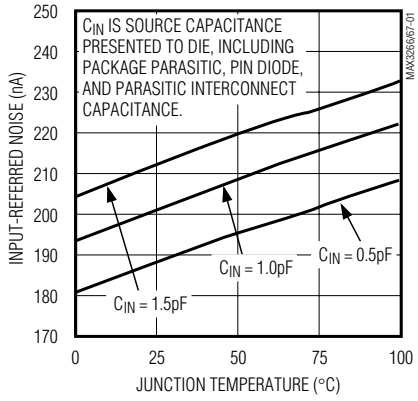
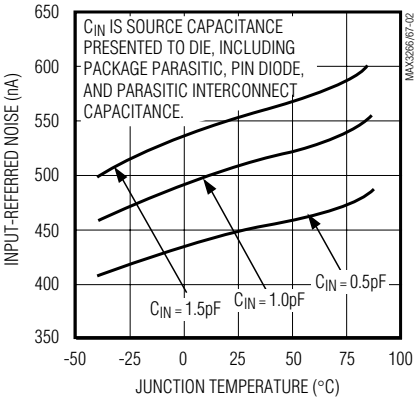
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, MAX3266/MAX3267 EV kit, source capacitance = 0.85pF, unless otherwise noted.)

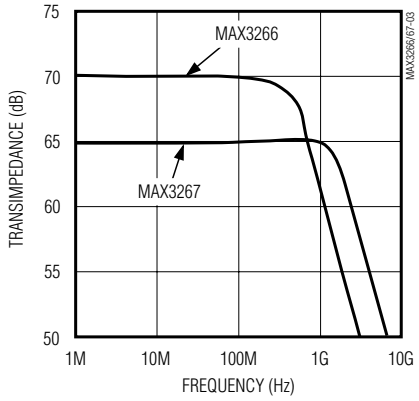
MAX3266
INPUT-REFERRED NOISE vs. TEMPERATURE



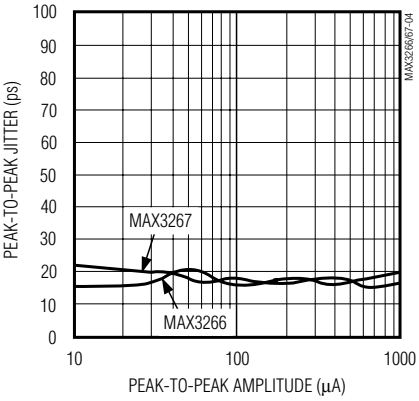
MAX3267
INPUT-REFERRED NOISE vs. TEMPERATURE



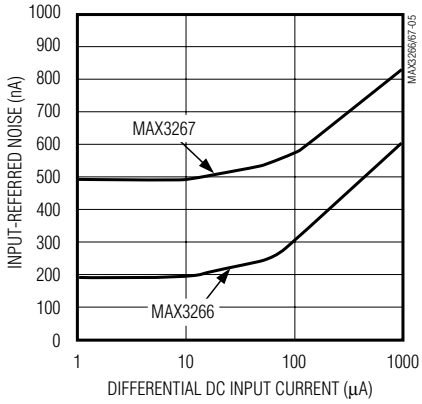
FREQUENCY RESPONSE



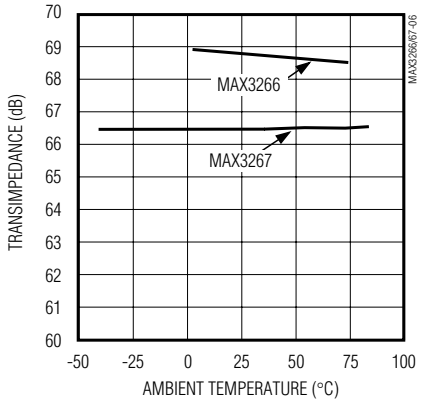
DETERMINISTIC JITTER
vs. INPUT AMPLITUDE



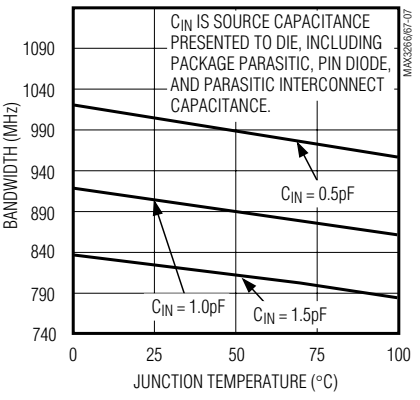
INPUT-REFERRED RMS NOISE CURRENT
vs. DC INPUT CURRENT



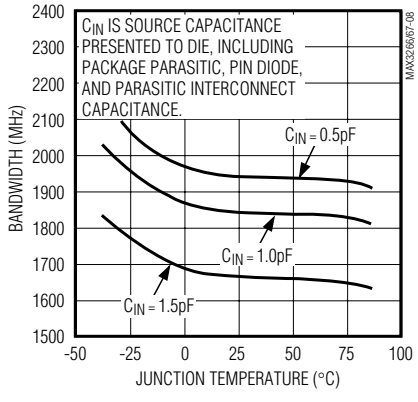
SMALL-SIGNAL TRANSIMPEDANCE
vs. TEMPERATURE



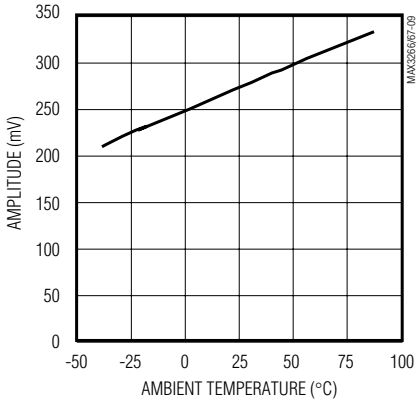
MAX3266
BANDWIDTH vs. TEMPERATURE



MAX3267
BANDWIDTH vs. TEMPERATURE



OUTPUT AMPLITUDE vs. TEMPERATURE

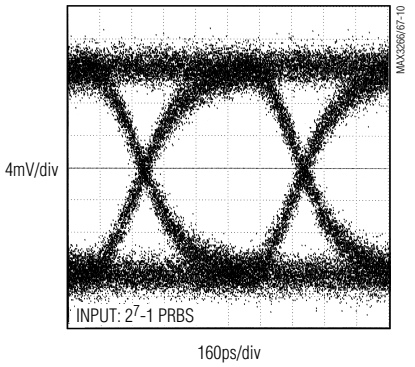


1.25Gbps/2.5Gbps, +3V to +5.5V, Low-Noise Transimpedance Preamplifiers for LANs

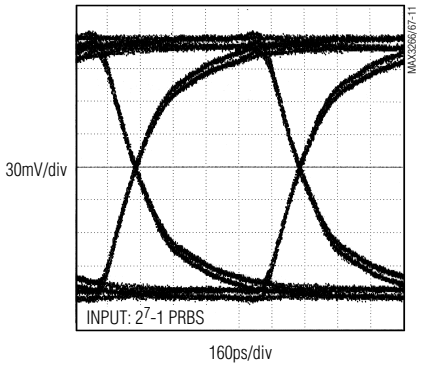
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, MAX3266/MAX3267 EV kit, source capacitance = 0.85pF, unless otherwise noted.)

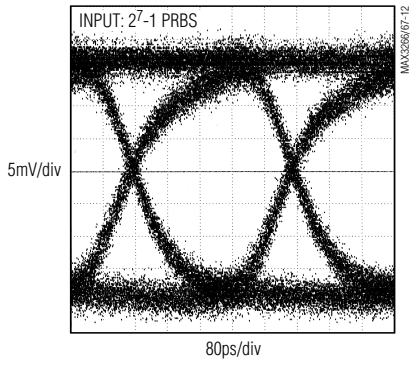
EYE DIAGRAM (INPUT = 10µAp-p)



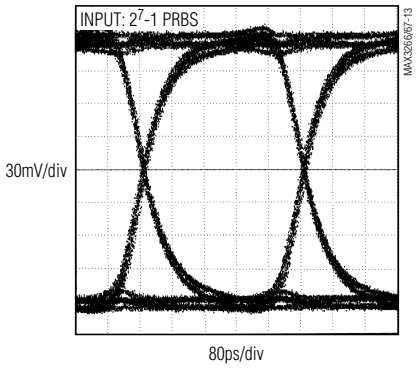
EYE DIAGRAM (INPUT = 1mAp-p)



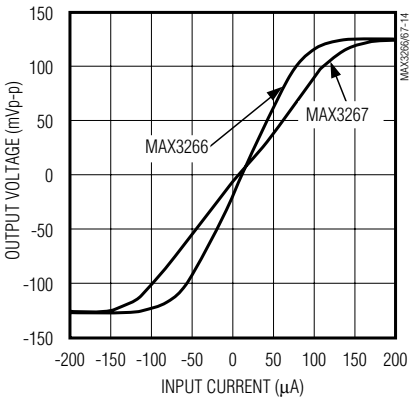
EYE DIAGRAM (INPUT = 20µAp-p)



EYE DIAGRAM (INPUT = 1mAp-p)



DC TRANSFER FUNCTION



Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Supply Voltage
2	N.C.	No Connection. Not internally connected.
3	IN	Amplifier Input
4	FILTER	Provides bias voltage for the photodiode through a 1.5kΩ resistor to V_{CC}. When grounded, this pin disables the DC Cancellation Amplifier to allow a DC path from IN to OUT+ and OUT- for testing.
5	GND	Ground
6	OUT-	Inverting Output. Current flowing into IN causes V_{OUT-} to decrease.
7	OUT+	Noninverting Output. Current flowing into IN causes V_{OUT+} to increase.
8	GND	Ground

1.25Gbps/2.5Gbps, +3V to +5.5V, Low-Noise Transimpedance Preamplifiers for LANs

Detailed Description

The MAX3266 is a transimpedance amplifier designed for 1.25Gbps fiber optic applications. Figure 2 is a functional diagram of the MAX3266, which comprises a transimpedance amplifier, a voltage amplifier, an output buffer, an output filter, and a DC cancellation circuit.

The MAX3267, a transimpedance amplifier designed for 2.5Gbps fiber optic applications, shares similar architecture with the MAX3266.

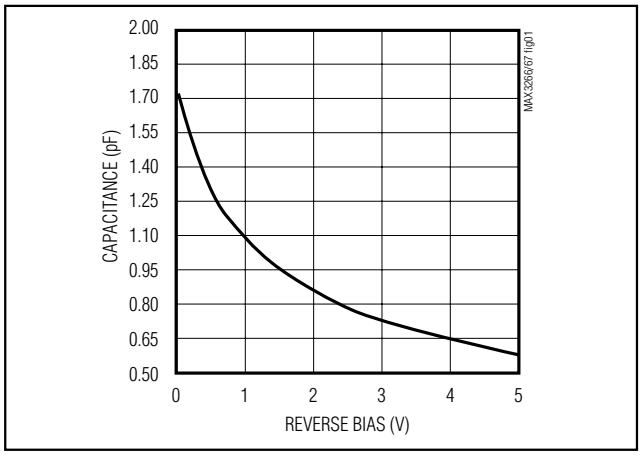


Figure 1. Typical Photodiode Capacitance vs. Bias Voltage

Transimpedance Amplifier

The signal current at the input flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage with gain of approximately 2.2kΩ (1.0kΩ for MAX3267). Schottky diodes clamp the output voltage for large input currents, as shown in Figure 3.

Voltage Amplifier

The voltage amplifier converts single-ended signals to differential signals and introduces a voltage gain.

Output Buffer

The output buffer provides a reverse-terminated voltage output. The buffer is designed to drive a 100Ω differential load between OUT+ and OUT-. The output current is divided between internal 50Ω load resistors and the external load resistor. In the typical operating circuit, this creates a voltage-divider with gain of 1/2. The MAX3266 can also be terminated with higher output impedances, which increases gain and output voltage swing.

For optimum supply-noise rejection, the MAX3266 should be terminated with a differential load. If a single-ended output is required, the unused output should be similarly terminated. The MAX3266 will not drive a DC-coupled, 50Ω grounded load.

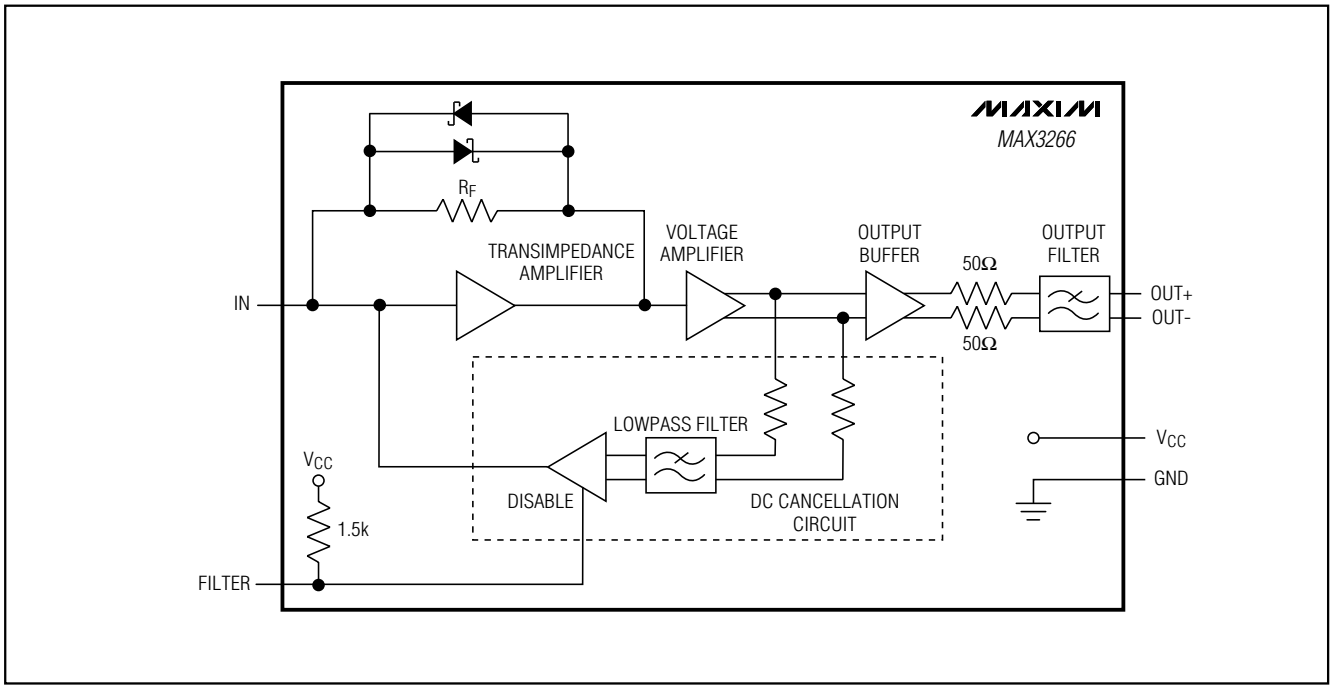


Figure 2. MAX3266 Functional Diagram

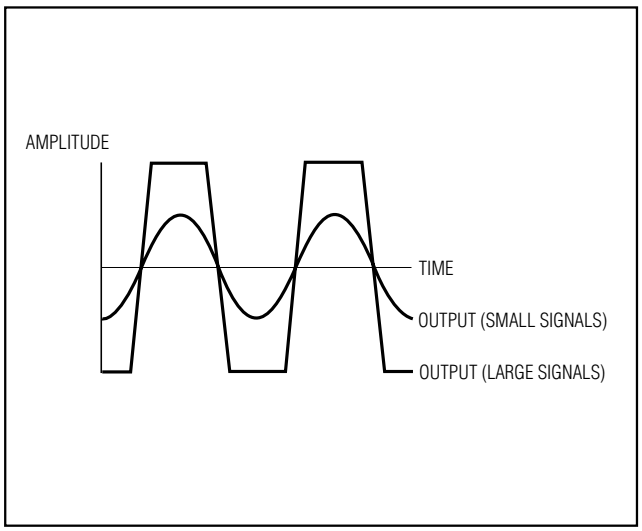


Figure 3. MAX3266 Limited Output

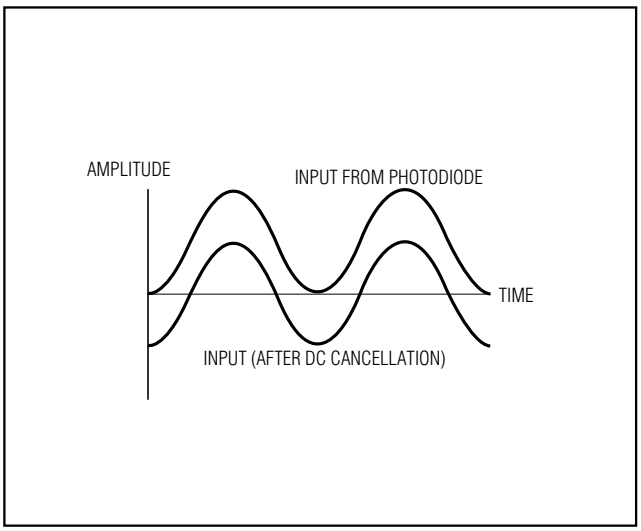


Figure 4. DC Cancellation Effect on Input

Output Filter

The MAX3266 includes a one-pole lowpass filter that limits the circuit bandwidth and improves noise performance.

DC Cancellation Circuit

The DC cancellation circuit uses low-frequency feedback to remove the DC component of the input signal (Figure 4). This feature centers the input signal within the transimpedance amplifier's linear range, thereby reducing pulse-width distortion on large input signals.

The DC cancellation circuit is internally compensated and therefore does not require external capacitors. This circuit minimizes pulse-width distortion for data sequences that exhibit a 50% duty cycle. A duty cycle significantly different from 50% will cause the MAX3266 to generate pulse-width distortion.

DC cancellation current is drawn from the input and creates noise. For low-level signals with little or no DC component, this is not a problem. Amplifier noise will increase for signals with significant DC component (see *Typical Operating Characteristics*).

Applications Information

Optical Power Relations

Many of the MAX3266 specifications relate to the input signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. Figure 5 shows relations that are helpful for converting optical power to input signal when designing with the MAX3266.

Optical power relations are shown in Table 1; the definitions are true if the average duty cycle of the input data is 50%.

Optical Sensitivity Calculation

The input-referred RMS noise current (I_N) of the MAX3266 generally determines the receiver sensitivity. To obtain a system bit error rate (BER) of 1E-12, the SNR ratio must always exceed 14.1. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log\left(\frac{14.1\ I_N\left(r_e + 1\right)}{2\rho\left(r_e - 1\right)}1000\right)\ \text{dBm}$$

Where ρ is the photodiode responsivity in A/W.

Input Optical Overload

The overload is the largest input that the MAX3266 accepts while meeting specifications. The optical overload can be estimated in terms of average power with the following equation:

$$\text{Overload} = 10\log\left(\frac{1\text{mA}}{2\rho}1000\right)\ \text{dBm}$$

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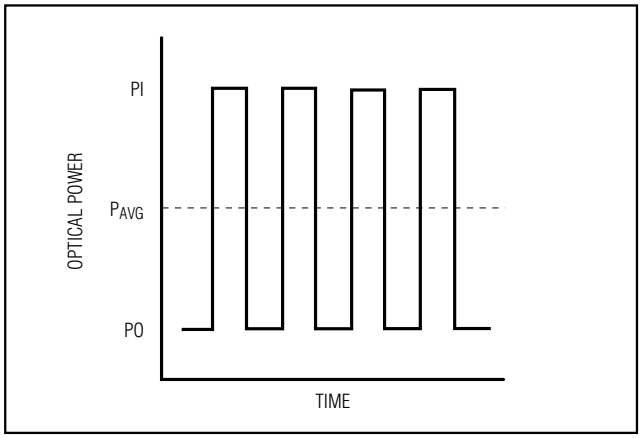


Figure 5. Optical Power Relations

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P0 + P1) / 2$
Extinction Ratio	r_e	$r_e = P1/P0$
Optical Power of a 1	P1	$P1 = 2P_{AVG} (r_e) / (r_e + 1)$
Optical Power of a 0	P0	$P0 = 2P_{AVG} / (r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVG} (r_e) / (r_e + 1)$

Optical Linear Range

The MAX3266 has high gain, which limits the output when the input signal exceeds 30µAp-p (40µAp-p for MAX3267). The MAX3266 operates in a linear range for inputs not exceeding:

$$\text{Linear Range} = 10\log\left(\frac{30\mu A(r_e + 1)}{2\rho(r_e - 1)}1000\right) \text{ dBm}$$

Layout Considerations

Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and power planes is recommended. Connect the GND pins to the ground plane with the shortest possible traces.

Noise performance and bandwidth will be adversely affected by capacitance at the IN pin. Minimize capacitance on this pin and select a low-capacitance photodiode. Assembling the MAX3266 in die form using chip and wire technology provides the best possible performance. Figure 6 shows a suggested layout for a TO header.

The SO package version of the MAX3266 is offered as an easy way to characterize the circuit and become familiar with the circuit's operation, but it does not offer optimum performance. When using the SO version of the MAX3266, the package capacitance adds approximately 0.3pF at the input. The PC board between the MAX3266 input and the photodiode also adds parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it.

Photodiode Filter

Supply voltage noise at the cathode of the photodiode produces a current $I = C_{PD}\ \Delta V/\Delta t$, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance.) The filter resistor of the MAX3266, combined with an external capacitor, can be used to reduce this noise (see the *Typical Application Circuit*). Current generated by supply noise voltage is divided between C_{FILTER} and C_{PD}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(C_{FILTER})$$

If the amount of tolerable noise is known, the filter capacitor can be easily selected:

$$C_{FILTER} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(I_{NOISE})$$

For example, with maximum noise voltage = 100mVp-p, C_{PD} = 0.85pF, R_{FILTER} = 1.5kΩ, and I_{NOISE} selected to be 100nA (1/2 of the MAX3266's input noise):

$$C_{FILTER} = (100mV)(0.85pF) / (1500\Omega)(100nA) = 570pF$$

Wire Bonding

For high current density and reliable operation, the MAX3266 uses gold metalization. Connections to the die should be made with gold wire only, using ball-bonding techniques. Wedge bonding is not recommended. Die thickness is typically 15mils (0.375mm).

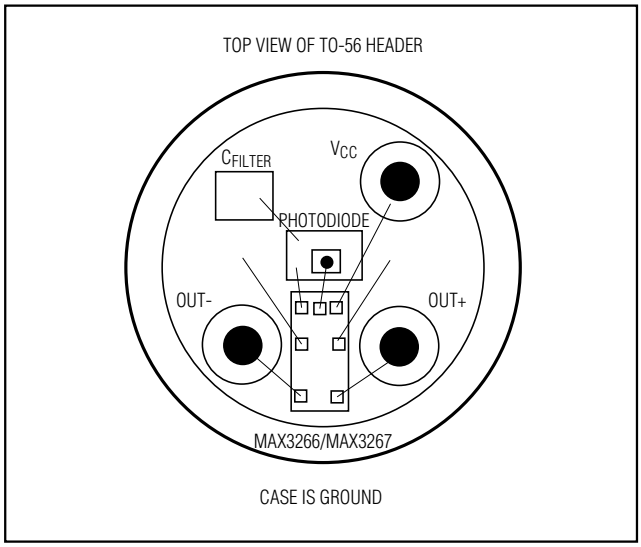
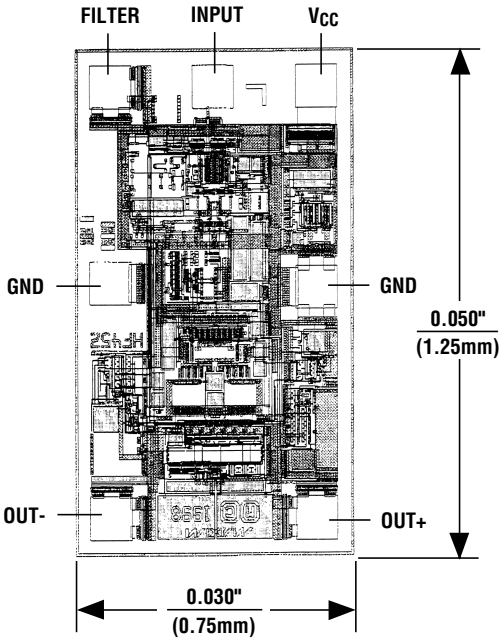


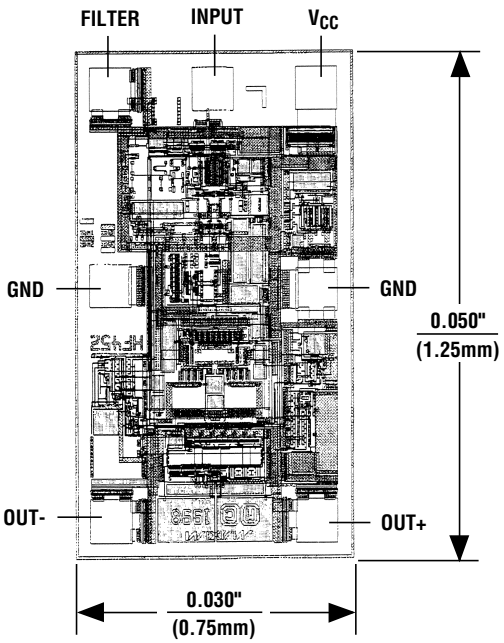
Figure 6. Suggested Layout for TO-56 Header

Chip Topographies

MAX3266



MAX3267

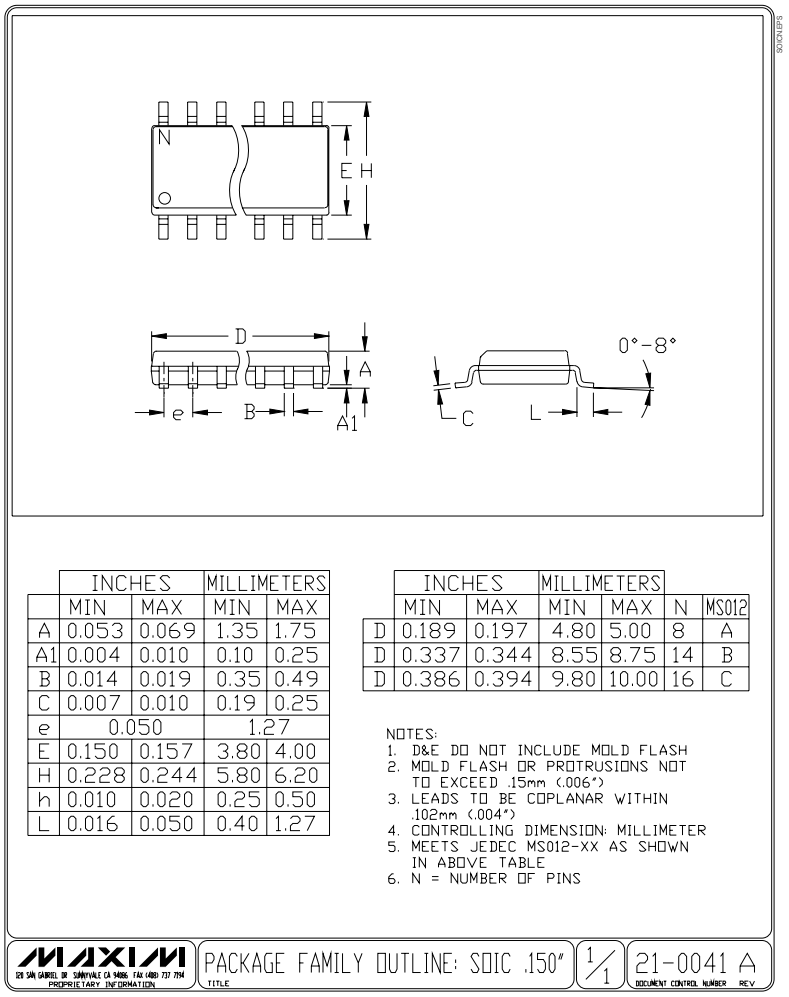


TRANSISTOR COUNT: 320

SUBSTRATE CONNECTED TO GND

1.25Gbps/2.5Gbps, +3V to +5.5V, Low-Noise Transimpedance Preamplifiers for LANs

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: SOIC .150" TITLE | 1/1 | 21-0041 A DOCUMENT CONTROL NUMBER REV.